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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	PAPER NUMBER
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,588	TANDJOENG, SOEPARTO	
	Examiner	Art Unit	
	Yolanda L. Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7,14-16,18-32,34 are rejected under 35 U.S.C. 102(e) as being anticipated by Duesman et al. (USPN 6105152A). As per claim 1, Thatcher et al. discloses selecting a memory cell to be tested from a fringe region of an array of the memory device; and testing said selected memory cell using at least one test parameter that is different than a test parameter to be used for memory cells not in the fringe region in column 7, lines 15-48.

3. As per claim 2, Duesman et al. discloses wherein said act of selecting comprises selecting the memory cell from a region that is adjacent to a periphery of said array in column 7, lines 32-48.

4. As per claim 3, Duesman et al. discloses wherein said act of selecting comprises selecting the memory cell from a region that is adjacent to a folded bitline of said array in column 7, lines 32-48.

5. As per claim 4, Duesman et al. discloses wherein said at least one parameter is a first voltage level that is different from a voltage level used to test memory cells not in the fringe in column 7, lines 32-48.

6. As per claim 5, Duesman et al. discloses wherein said first voltage level is different than a supply voltage in column 7, lines 32-48.

7. As per claim 6, Duesman et al. discloses The method of claim 5, where said first voltage level is less than approximately 2.5V in column 7, lines 15-48.

8. As per claim 7, Duesman et al. discloses wherein said act of testing comprises testing said selected memory cell using at least one test parameter more demanding than said test parameter to be used for memory cells not in the fringe region in column 7, lines 15-48.

9. As per claim 14, Duesman et al. discloses identifying a first plurality of memory cells of said integrated circuit memory for testing; and determining if said first plurality of memory cells are weak cells in column 7, lines 15-48.

10. As per claim 15, Duesman et al. discloses wherein said act of determining comprises stressing said identified first plurality of memory cells to determine if they are weak cells in column 7, lines 15-48.

11. As per claim 16, Duesman et al. discloses wherein said act of stressing comprises applying a test voltage at a level below a test voltage used for other memory cells of said integrated circuit memory in column 7, lines 15-48.

12.

13. As per claim 18, Duesman et al. discloses wherein said first plurality of memory cells comprises memory cells located in a row adjacent to a top edge of said memory in column 7, lines 32-48.

14. As per claim 19, Duesman et al. discloses wherein said first plurality of memory cells comprises memory cells located in a row adjacent to a bottom edge of said memory in column 7, lines 32-48.

15. As per claim 20, Duesman et al. discloses wherein said first plurality of memory cells comprises memory cells located in a row adjacent to a folded digitline of said memory in column 7, lines 32-48.

16. As per claim 21, Duesman et al. discloses wherein said first plurality of memory cells comprises memory cells located in a column adjacent to at least one of a right edge and a left edge of said memory in column 7, lines 32-48.

17. As per claim 22, Duesman et al. discloses wherein said first plurality of memory cells comprises memory cells located in at least one of a first and second row of memory adjacent to an edge of said memory in column 7, lines 32-48.

18. As per claim 23, Duesman et al. discloses wherein said second row of memory is adjacent to said first row of memory in column 7, lines 32-48.

19. As per claim 24, Duesman et al. discloses wherein said second row of memory is not adjacent to said first row of memory in column 7, lines 32-48.

20. As per claim 25, Duesman et al. discloses wherein said edge of said memory is a top edge of said memory in column 7, lines 32-48.

21. As per claim 26, Duesman et al. discloses wherein said edge of said memory is a bottom edge of said memory in column 7, lines 32-48.

22. As per claim 27, Duesman et al. discloses wherein said first plurality of memory cells comprises memory cells located in at least one of a first and second column of memory adjacent to an edge of said memory in column 7, lines 32-48.

23. As per claim 28, Duesman et al. discloses wherein said second column of memory is adjacent to said first column of memory in column 7, lines 32-48.

24. As per claim 29, Duesman et al. discloses wherein said second column of memory is not adjacent to said first column of memory in column 7, lines 32-48.

25. As per claim 30, Duesman et al. discloses wherein said edge of said memory is a right edge of said memory in column 7, lines 32-48.

26. As per claim 31, Duesman et al. discloses wherein said edge of said memory is a left edge of said memory in column 7, lines 32-48.

27. As per claim 32, Duesman et al. discloses test control circuitry; and connecting circuitry that connects the test control circuitry to a memory device under test; the test control circuitry providing signals through the connecting circuitry to: select a memory cell to be tested from a fringe region of an array of the memory device; and test said selected memory cell using at least one test parameter that is different than a test parameter to be used for memory cells not in the fringe region in column 5, lines 1-9; column 7, lines 15-48.

28. As per claim 34, Duesman et al. discloses test control circuitry; and connecting circuitry that connects the test control circuitry to a memory device under test; the test

control circuitry providing signals through the connecting circuitry to: identify a first plurality of memory cells of said integrated circuit memory for testing; and determine if said first plurality of memory cells are weak cells in column 5, lines 1-9; column 7, lines 15-48.

Claim Rejections - 35 USC § 103

29. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. Claims 8-10,17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duesman et al. (USPN 6754116B2) in view of McClure (USPN 6006339A).

31. As per claim 8, Duesman et al. fails to explicitly state wherein said at least one parameter is a first write recovery time that is different from a second write recovery time used to test memory cells not in the fringe.

McClure discloses this limitation in column 3, lines 24-31.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have at least one parameter is a first write recovery time that is different from a second write recovery time used to test memory cells not in the fringe. A person of ordinary skill in the art would have at least one parameter is a first write recovery time that is different from a second write recovery time used to test memory cells not in the fringe because the shorter write time allows for determination of accurately written data.

32. As per claim 9, Duesman et al. fails to explicitly state wherein said first write recovery time is shorter than approximately 12 ns.

McClure discloses this limitation in column 3, lines 24-31.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have at least one parameter is a first write recovery time that is different from a second write recovery time used to test memory cells not in the fringe. A person of ordinary skill in the art would have at least one parameter is a first write recovery time that is different from a second write recovery time used to test memory cells not in the fringe because the shorter write time allows for determination of accurately written data.

33. As per claim 10, Duesman et al. fails to explicitly wherein said first write recovery time is between approximately 79-96% of the second write recovery time.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said first write recovery time is between approximately 79-96% of the second write recovery time. A person of ordinary skill in the art would have said first write recovery time is between approximately 79-96% of the second write recovery time because the shorter write time allows for determination of accurately written data.

34. As per claim 17, Duesman et al. fails to explicitly state wherein said act of stressing comprises applying a shorter than standard write release time.

McClure discloses this limitation in column 3, lines 24-31.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have where said first data is provided at a shorter write release time. A person of ordinary skill in the art would have where said first data is provided at a shorter write release time because the shorter write time allows for determination of accurately written data.

35. Claims 11-13,33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Janik et al. (USPN 6754116B2) in view of McClure (USPN 6006339A) in further view of Duesman et al.

36. As per claims 11,33, Janik et al. discloses selecting a column of a memory array of said memory device to be tested; selecting a row of said memory array to be tested; writing first data to each said memory cell in said memory array; activating said selected row for reading and writing; providing second data to a memory cell corresponding to said selected row and selected column, said second data being different from said first data; precharging said selected row for deactivating said selected row for reading and writing; activating said selected row for reading and writing; re-activating said selected row for reading and writing; reading test data from said memory cell; and determining if said test data is correct in column 8, line 57 – column 9, line 10.

Janik et al. fails to explicitly state where said first data is provided at a shorter write release time.

McClure discloses this limitation in column 3, lines 24-31.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have where said first data is provided at a shorter write

release time. A person of ordinary skill in the art would have where said first data is provided at a shorter write release time because the shorter write time allows for determination of accurately written data.

Janik et al. and McClure fail to explicitly state providing said selected column and row defining a memory cell in a fringe region of said memory array and said first data to said memory cell corresponding to said selected row and selected column, where said first data is provided at a lower voltage than supply voltage.

Duesman et al. discloses these limitations in column 7, lines 15-48.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have providing said selected column and row defining a memory cell in a fringe region of said memory array and said first data to said memory cell corresponding to said selected row and selected column, where said first data is provided at a lower voltage than supply voltage. A person of ordinary skill in the art would have providing said selected column and row defining a memory cell in a fringe region of said memory array and said first data to said memory cell corresponding to said selected row and selected column, where said first data is provided at a lower voltage than supply voltage because the selecting of memory cells allows for different cells to be tested and stressed by using different voltages in order to determine errors in the selected memory cells.

37. As per claim 12, Janik et al. discloses initializing the memory array for access and storage in column 8, lines 18-39.

38. As per claim 13, Janik et al. discloses loading a mode register associated with said memory array to establish the write mode in column 8, lines 18-39.

Claim Objections

39. Claims 32-34 are objected to because of the following informalities: In claims 32-34, 'comprising;' should be 'comprising:'. Appropriate correction is required.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Yolanda L Wilson
Examiner
Art Unit 2113